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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	10/708,268
Filing Date	02/20/2004
First Named Inventor	Praveen K. Samudrala
Art Unit	~~2816~~ 2819
Examiner Name	Unassigned
Attorney Docket Number	1372.136.PRC

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
OC	1	SAMUDRALA, PRAVEEN KUMER ET AL., Selective Triple modular Redundancy for SEU Mitigation in FPGAs, pgs 1-3, No date	
OC	2	SAMUDRALA, PRAVEEN K. ET AL., Selective Triple Modular Redundancy (STMR) Based Single Event Upset (SEU) Tolerant Synthesis for FPGAs, pgs 1-26, 10/2004	
OC	3	SAMUDRALA, PRAVEEN K. ET AL., A Novel Technique for SEU Mitigation in Combinational Circuits Mapped to FPGA's, pgs 1-31. No Month 2001	
OC	4	CARMICHAEL, CARL, Triple Module Redundancy Design Techniques for Virtex FPGAs, XILINX, Nov. 1, 2001, pgs 1-37, XAPP197 (v1.0).	
OC	5	LABEL, KENNETH A. ET AL., Single-Event-Effect Mitigation from a System Perspective, IEEE Transactions on Nuclear Science, April 1996, 46-2, pp. 654-660	

Examiner Signature		Date Considered	12/29/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known	
Application Number	10/708,268
Filing Date	02/20/2004
First Named Inventor	Praveen K. Samudrala
Art Unit	~~2848~~ 2814
Examiner Name	Unassigned
Attorney Docket Number	1372.136.PRC

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 6,298,289	10/02/2001	Lloyd et al.	
	2	US- 4,964,126	10/16/1990	Musicus et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

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Sheet 2 of 2

Complete If Known	
Application Number	10/708,268
Filing Date	02/20/2004
First Named Inventor	Praveen K. Samudrala
Art Unit	~~2816~~ 2819
Examiner Name	Unassigned
Attorney Docket Number	1372.136.PRC

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
DC	1	EDUARDO AUGUSTO BEZERRA ET AL., Improving Reconfigurable Systems Reliability by Combining Periodical Test and Redundancy Techniques: A Case Study, pp. 1-10 No date	
DC	2	ZOLTAN MEGGYESI ET AL., FPGA Design in the Presence of Single Event Upsets, CERN, Geneva, Switerland. pp. 1-4, no date.	
DC	3	Single Event Upset (SEU) Mitigation by Virtual Triple Modular Redundancy (TMR) in Design Reduces Manufacturing Cost and Lowers Power, Alternative System Concepts, Inc., pg 1-7, No date	
DC	4	EARL FULLER ET AL., Radiation Testing Update, SEU Mitigation, and Availability Analysis of the Virtex FPGA for Space Reconfigurable Computing, pg. 1-11, 9/2000	
DC	5	K. NIKOLIC ET AL., Fault-Tolerant Techniques for Nanocomputers, TNT2001, Sept. 3-7, 2001, Segovia, Spain, pp. 1-3	
DC	6	CARL CARMICHEAL ET AL., SEU MitigationTechniques for Virtex FPGAs in Space Application, pp. 1-11, ~~No date~~ 1999 Xilinx	
DC	7	PRAVEEN SAMUDRALA ET AL., Single Event Upsets and Mitigation Technigues: A Survey, pages 1-15, no date	
DC	8	SRINIVAS KATKOORI, SEU Tolerant Design Techniques for Space Based RC Implementations, IR & D Project, March 28, 2001, pp. 1-2	
DC	9	PRAVEEN K. SAMUDRALA, Synthesis of SEU Tolerant FPGAs, January 22, 2003, pages 1-53.	

Examiner Signature		Date Considered	12/29/04

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